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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/617,040 | 07/11/2003 | Yutaka Ito | Q76480 | 3063 |

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

| EXAMINER | |
|---|---|
| CHAUDRY, MUJTABA M | |
| ART UNIT | PAPER NUMBER |
| 2133 | |

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/617,040 | ITO ET AL. | |
| | Examiner | Art Unit | |
| | Mujtaba K. Chaudry | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *1,6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on July 11, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the Examiner, however there are no translations submitted with the foreign documents.

### *Oath/Declaration*

The Oath filed July 11, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

### *Drawings*

The drawings are objected to because:

- Figure 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page

header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- Figure 18 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- Figure 19 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37

CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

## *Specification*

Applicant is reminded of the proper language and format for an abstract of the disclosure.

> ***The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.***

> ***The language should be clear and concise and should not repeat information given in the title or claim(s). It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.***

The abstract of the disclosure is objected to because in line 2 it is not clear what is being stated, "...capable of correcting efficiently bits having a low error rate..."

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Objections*

Claim 1 is objected to because of the following informalities:

- The term "where" in lines 3 and 4 should be replaced with "wherein".

Appropriate correction is required.

Claim 6 is objected to because of the following informalities:

- The term "is" in line 3 should be replaced with "are".

Appropriate correction is required.

Claim 9 is objected to because of the following informalities:

- The term "where" in lines 3 and 4 should be replaced with "wherein".
- The term "cord" in line 9 should be "code".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the last paragraph it is not clear what the redundant correcting process is being combined with.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the last line, the thought is not complete. What is "made"?

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the last line, the thought is not complete. What is "made"?

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemae (USPN 4688219) further in view of Fifield (USPN 5307356).

As per claim 1, Takemae substantially teaches to check for errors in a memory using parity checking techniques and to correct the detected errors using redundant memory cells. Takemae teaches a semiconductor memory device (col. 1, line 65) with a parity portion and a redundant portion (col. 1, lines 66-68). Takemae teaches an error correcting circuit (col. 2, lines 14-15) to perform error correction. Takemae also teaches to combine the redundant correcting and parity checking process as stated in the present application.

Takemae does not explicitly teach the error correction circuit to use a Hamming code for the correction process as stated in the present application.

However, Fifield, in an analogous art, substantially teaches (abstract) a DRAM which includes an on-chip ECC system. Particularly, Fifield teaches (col. 6, lines 4-23) the error correction circuit to use Hamming code. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Hamming code for the correction process in the error correction circuit within the method and apparatus of Takemae. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by utilizing a Hamming code within the error correction circuitry would have improved the error detection and correction capability.

As per claim 2, Takemae substantially teaches, in view of above rejections, (col. 1, lines 17-22) when a defective memory cell is selected to be read, the redundant memory cell is actually read in place of the defective memory cell, so that the correct data can be read.

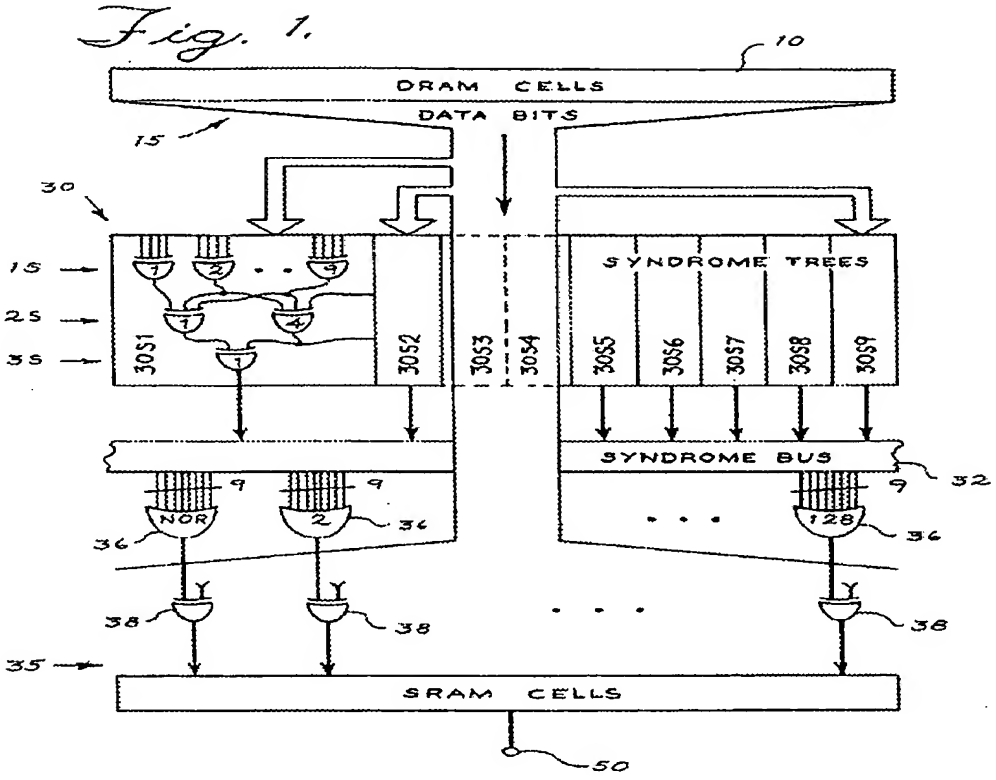
As per claim 3, Fifield substantially teaches, in view of above rejections, (col. 6, lines 2-23) a Hamming code used in the error correcting circuit which is able detect a double error or correct a single error. The Examiner would like to point out that Hamming codes are known to

have such standardized properties and in fact all error-correcting codes are limited in correcting detected errors. Furthermore, if the code word is found to have more errors than that are correctable, usually it has to be replaced with a redundant code word.

As per claim 4, Takemae substantially teaches, in view of above rejections, (col. 2) the error correcting circuit includes a data selector, operatively connected to the memory cell array, for receiving read data from a plurality of memory cells including a selected memory cell. The data selection also selectively outputs a part of the read data which forms horizontal and vertical parity-checking groups corresponding to a parity-checking two-dimensional virtual matrix. A vertical parity generator and a horizontal parity generator are connected to the data selector, for generating a vertical parity and a horizontal parity of the data group, respectively. In addition, a parity storing memory for storing a previously determined vertical parity and a previously determined horizontal parity are included along with a comparator connected to the vertical and horizontal parity generators and to the parity storing memory. The comparator compares the outputs of the inhibit and parity generating circuit with the previously determined vertical and horizontal parities so as to correct an error in the read data.

As per claims 5-7, Fifield substantially teaches, in view of above rejections, (Figure 1) syndrome generator 30S1, each generator (or "syndrome tree") is made up of three stage exclusive-OR (XOR) logic trees. The first stage 1S of the logic tree is made up of a first set of four-input XOR gates; the second stage 2S is made up of approximately four four-input XOR gates; and the final stage 3S is a single four-input XOR gate. Note that the syndrome generators 30S1-30S9 have different numbers of inputs (specifically 51, 59, 59, 59, 55, 59, 60, 47, and 56 respectively) to optimize the interconnect wiring layout. The three stages of XOR of one

syndrome generator provide the parity of a subset of the one hundred and twenty eight data bits. This generated parity bit is then compared to a corresponding one of the stored check bits for that error correction word. The comparison operation, which is the XOR of a specific subset of PDL lines 15 and their corresponding stored check bits is executed by 1S, 2S and 3S. For the purposes of illustration, assume the arrowhead going into bus 32 is the result of this XOR operation. This XOR result is referred to as a syndrome bit, which is coupled to a respective line of a syndrome bus 32. The syndrome bus 32 is 18 bits wide (it carries the true and complement of each of the 9 syndrome bits). The inputs to the first stage S1 of each syndrome generator 30S1- 30S9 are subsets of the 128 data bits. Each syndrome generator receives a unique set of data bits, in accordance with the error correction code requirements. In other words, these XOR inputs are wired to calculate the parity of selected subsets of the 128-bit data word according to a parity check matrix defining the error correction code used.




As per claim 8, Fifield substantially teaches, in view of above rejections, (col. 3, lines 37-38) both the error correction circuitry and the redundant circuitry are on the same memory chip.

As per claim 9, Takemae substantially teaches to check for errors in a memory using parity checking techniques and to correct the detected errors using redundant memory cells. Takemae teaches a semiconductor memory device (col. 1, line 65) with a parity portion and a redundant portion (col. 1, lines 66-68). Takemae teaches an error correcting circuit (col. 2, lines 14-15) to perform error correction. Takemae also teaches to combine the redundant correcting and parity checking process as stated in the present application.

Takemae does not explicitly teach the error correction circuit to use a Hamming code for the correction process as stated in the present application.

However, Fifield, in an analogous art, substantially teaches (abstract) a DRAM which includes an on-chip ECC system. Particularly, Fifield teaches (col. 6, lines 4-23) the error correction circuit to use Hamming code. Fifield also teaches the code length to be less than 72 (col. 2, lines 10-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Hamming code for the correction process in the error correction circuit within the method and apparatus of Takemae. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by utilizing a Hamming code within the error correction circuitry would have improved the error detection and correction capability.

As per claim 10, Takemae substantially teaches, in view of above rejections, (col. 1, lines 17-22) when a defective memory cell is selected to be read, the redundant memory cell is actually read in place of the defective memory cell, so that the correct data can be read.

As per claim 11, Fifield substantially teaches, in view of above rejections, (col. 6, lines 2-23) a Hamming code used in the error correcting circuit which is able detect a double error or correct a single error. The Examiner would like to point out that Hamming codes are known to have such standardized properties and in fact all error-correcting codes are limited in correcting detected errors. Furthermore, if the code word is found to have more errors than that are correctable, usually it has to be replaced with a redundant code word.

As per claims 12-15, Fifield substantially teaches, in view of above rejections, (Figure 1) syndrome generator 30S1, each generator (or "syndrome tree") is made up of three stage exclusive-OR (XOR) logic trees. The first stage 1S of the logic tree is made up of a first set of four-input XOR gates; the second stage 2S is made up of approximately four four-input XOR

gates; and the final stage 3S is a single four-input XOR gate. Note that the syndrome generators 30S1-30S9 have different numbers of inputs (specifically 51, 59, 59, 59, 55, 59, 60, 47, and 56 respectively) to optimize the interconnect wiring layout. The three stages of XOR of one syndrome generator provide the parity of a subset of the one hundred and twenty eight data bits. This generated parity bit is then compared to a corresponding one of the stored check bits for that error correction word. The comparison operation, which is the XOR of a specific subset of PDL lines 15 and their corresponding stored check bits is executed by 1S, 2S and 3S. For the purposes of illustration, assume the arrowhead going into bus 32 is the result of this XOR operation. This XOR result is referred to as a syndrome bit, which is coupled to a respective line of a syndrome bus 32. The syndrome bus 32 is 18 bits wide (it carries the true and complement of each of the 9 syndrome bits). The inputs to the first stage S1 of each syndrome generator 30S1- 30S9 are subsets of the 128 data bits. Each syndrome generator receives a unique set of data bits, in accordance with the error correction code requirements. In other words, these XOR inputs are wired to calculate the parity of selected subsets of the 128-bit data word according to a parity check matrix defining the error correction code used.

As per claim 16, Fifield substantially teaches, in view of above rejections, (col. 3, lines 37-38) both the error correction circuitry and the redundant circuitry are on the same memory chip.

*Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
AU 2133
January 11, 2006